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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/829,235	04/22/2004	Takashi Ohtsuka	63979-042	7116
7590 05/23/2005 McDERMOTT, WILL & EMERY 600 13th Street, N.W. Washington, DC 20005-3096			EXAMINER LE, THONG QUOC	
			ART UNIT 2827	PAPER NUMBER

DATE MAILED: 05/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<p align="center"><b>Office Action Summary</b></p>	<b>Application No.</b> 10/829,235	<b>Applicant(s)</b> OHTSUKA ET AL.	
	<b>Examiner</b> Thong Q. Le	<b>Art Unit</b> 2827	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-19 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 4-19 is/are allowed.
- 6) ☒ Claim(s) 1 and 2 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |  |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                                  | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)            |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____  |

**DETAILED ACTION**

1. Amendment filed on 4/14/2005 has been entered.
2. Claims 1-19 are presented for examination.

***Response to Arguments***

3. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-2 are rejected under 35 U.S.C. 102(e) as being anticipated by Yokozeki (U.S. Patent No. 6,738,281)

Regarding claims 1-2, Yokozeki discloses a non-volatile memory cell (Figure 1) comprising:

a latch circuit (2) which comprises a first node (N) and a second node (NX) and latches complementary data set in the first node and second node;

a first switching element (4a) which connects the first node to a first data input/output line (BL) ;

a second switching element (4b) which connects the second node to a second data input/output line (BLX);

a first ferroelectric capacitor (3a) which connects the second data input/output line to the first node; and

a second ferroelectric capacitor (3b) which connects the first data input/output line to the second node.

More specifically, Yokozeki disclose in which the latch circuit (figure 1) comprises a first inverter and a second inverter (1a, 1b);

the first inverter (1a) comprising a first transistor and a second transistor which complement each other and are serially connected between a power line and ground (Figure 1);

the second inverter (1b) comprising a third transistor and a fourth transistor which complement each other and are serially connected between the power line and ground (Figure 1) ; the first and second transistors each having a gate and a drain, the gates of the first and second transistors being connected to the first node and the drains of the first and second transistors being connected to the second node; and the third and

fourth transistors each having a gate and a drain, the gates of the third and fourth transistors being connected to the second node and the drains of the third and fourth transistors being connected to the first node (Figure 1).

***Allowable Subject Matter***

6. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 3 includes allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Yokozeki (U.S. Patent No. 6,738,281), and others, does not teach the claimed invention having a resistance value of the first resistor being higher than the ON-resistance value of the first transistor.

7. Claims 4-19 are allowed.

Claims 4-19 includes allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Yokozeki (U.S. Patent No. 6,738,281), and others, does not teach the claimed invention having a method and an apparatus of a non-volatile memory device having a first ferroelectric capacitor and second ferroelectric capacitor select element which are serially connected between the second data input/output line and the first node.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai V. Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thong Q. Le  
Primary Examiner  
Art Unit 2827

**THONG LEI  
PRIMARY EXAMINER**